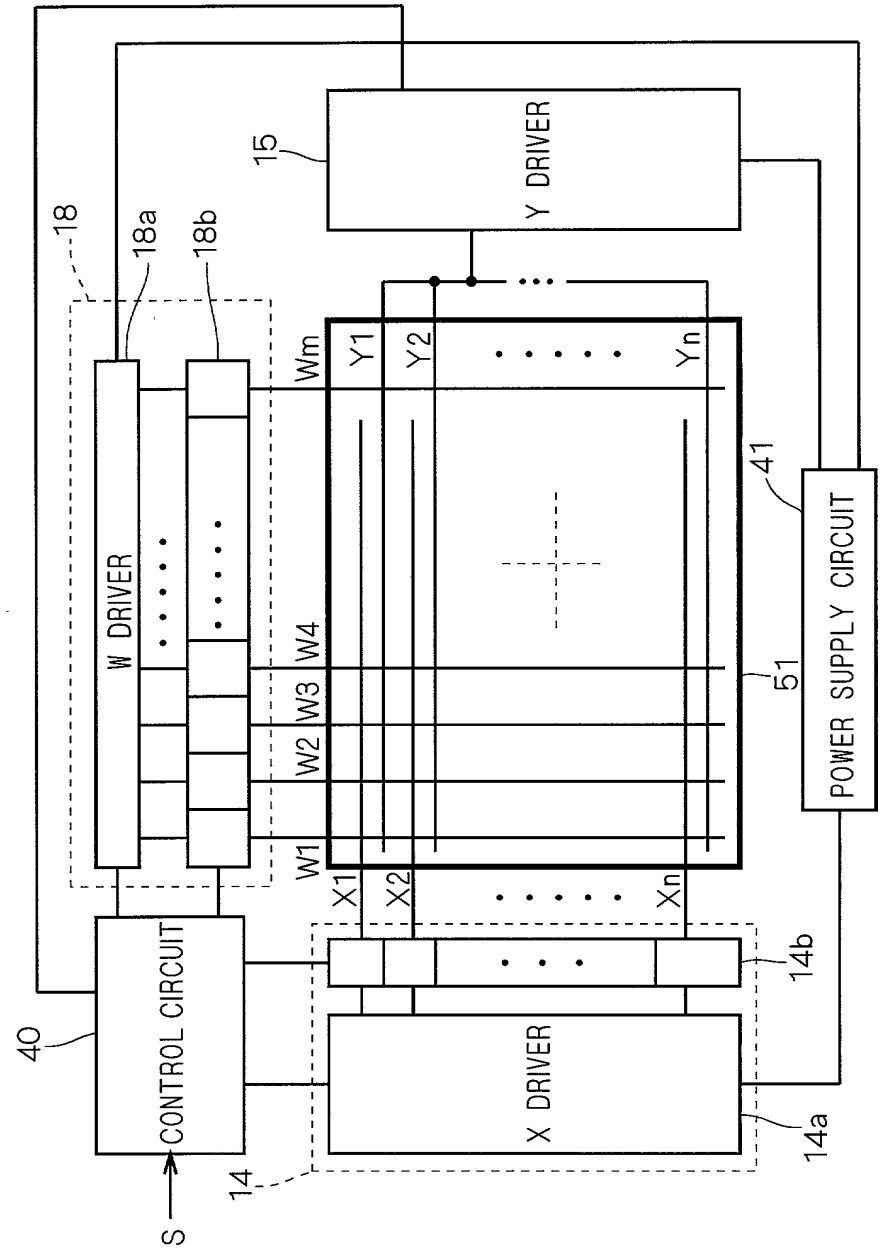

50
15
Y DRIVER
18
18a
18b
W DRIVER
Wm
W4
W3
W2
W1
Y1
Y2
Yn
X1
X2
Xn
41
POWER SUPPLY CIRCUIT
51
14b
X DRIVER
14a
40
CONTROL CIRCUIT
14
S

FIG. 1

FIG. 2

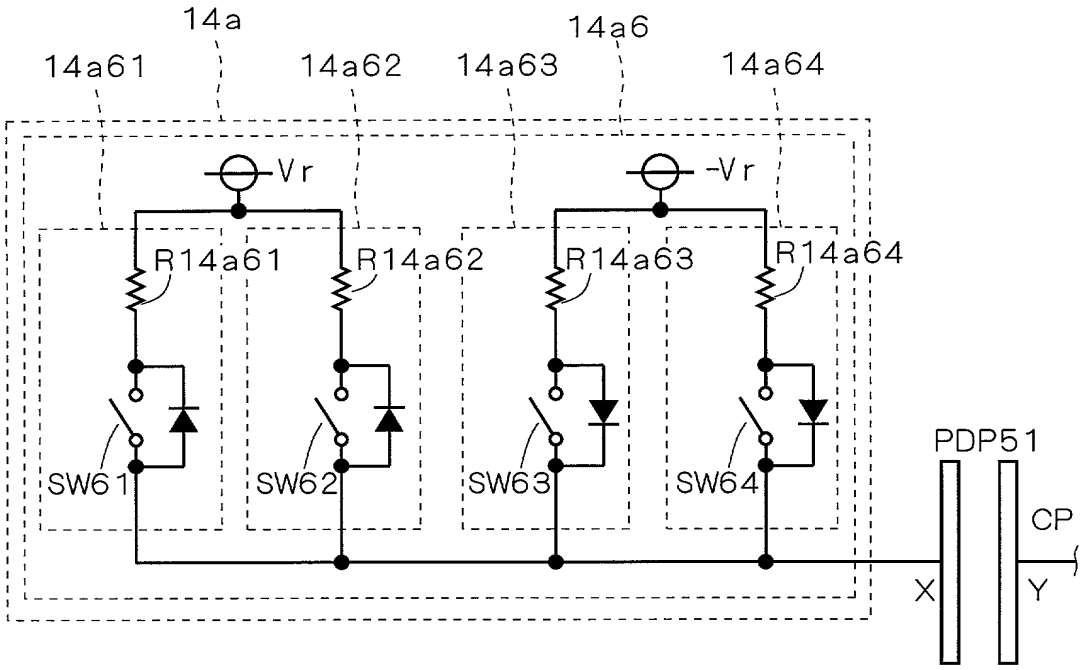

14a
14a61
14a62
14a63
14a6
14a64
Vr
-Vr
R14a61
R14a62
R14a63
R14a64
SW61
SW62
SW63
SW64
PDP51
CP
X
Y

FIG. 3

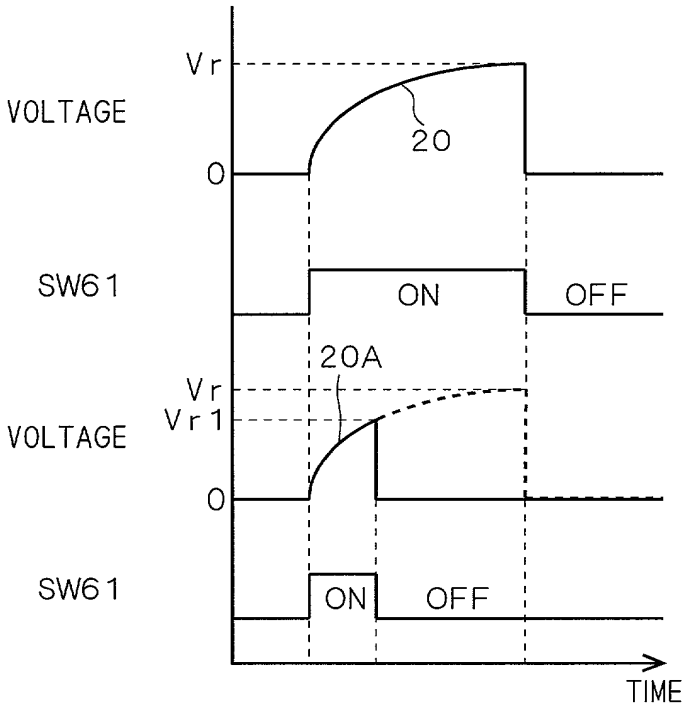

VOLTAGE
Vr
0
20
SW61
ON
OFF
20A
Vr
Vr1
VOLTAGE
0
SW61
ON
OFF
TIME

FIG. 4

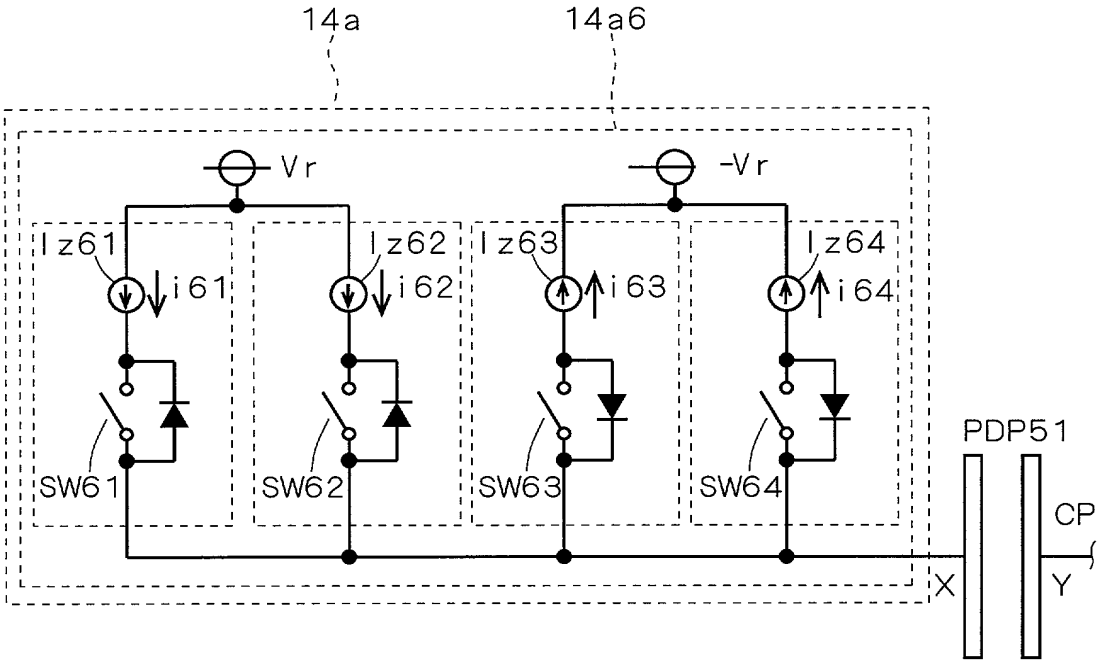

14a
14a6
Vr
-Vr
Iz61
Iz62
Iz63
Iz64
i61
i62
i63
i64
SW61
SW62
SW63
SW64
PDP51
CP
X
Y

FIG. 5

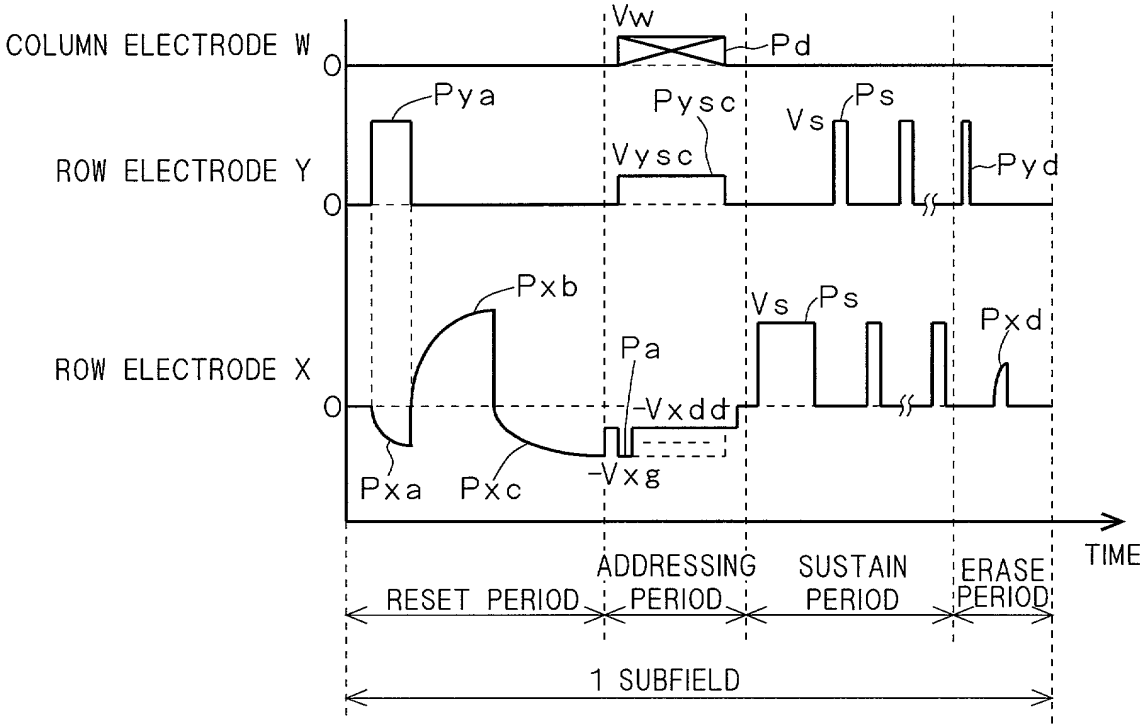

COLUMN ELECTRODE W
ROW ELECTRODE Y
ROW ELECTRODE X
0
Vw
Pd
Pya
Pysc
Vysc
Vs
Ps
Pyd
Pxb
Pa
-Vxdd
Pxd
Pxa
Pxc
-Vxg
TIME
RESET PERIOD
ADDRESSING PERIOD
SUSTAIN PERIOD
ERASE PERIOD
1 SUBFIELD

FIG. 6

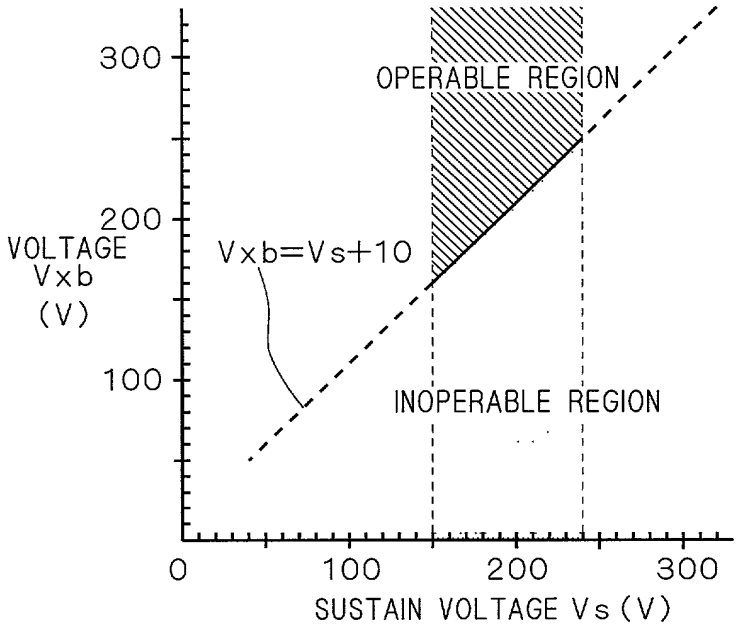

300
200
100
VOLTAGE
Vxb
(V)
OPERABLE REGION
Vxb=Vs+10
INOPERABLE REGION
0
100
200
300
SUSTAIN VOLTAGE Vs (V)

FIG. 7

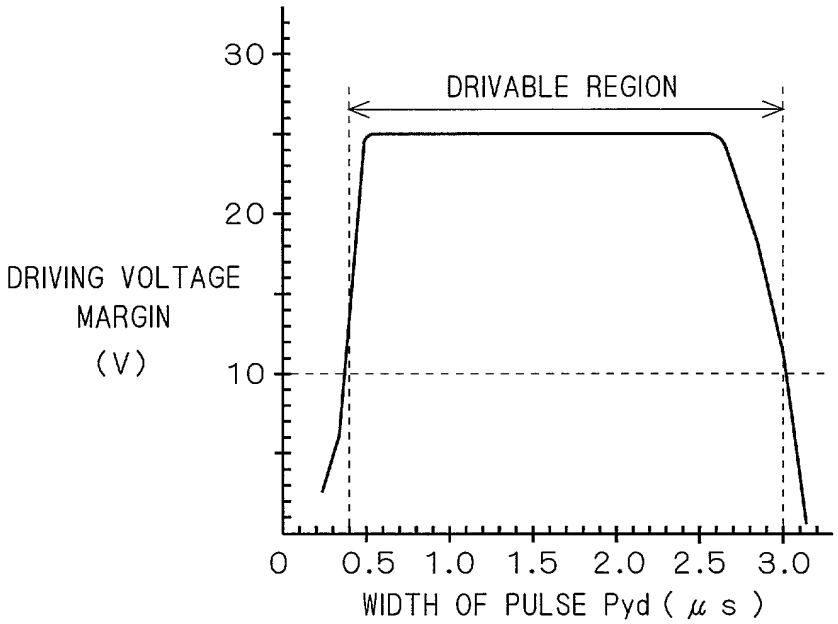

30
20
10
DRIVING VOLTAGE
MARGIN
(V)
DRIVABLE REGION
0
0.5
1.0
1.5
2.0
2.5
3.0
WIDTH OF PULSE Pyd (μ s)

FIG. 8

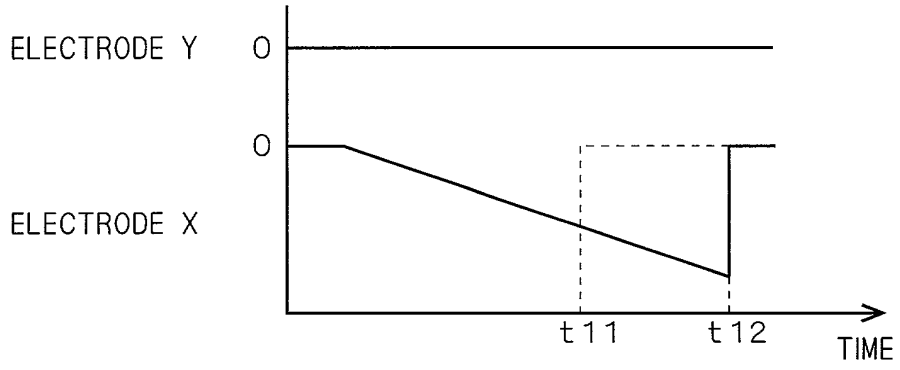


FIG. 9

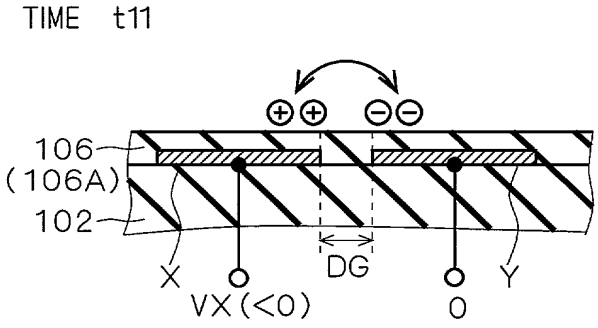


FIG. 10

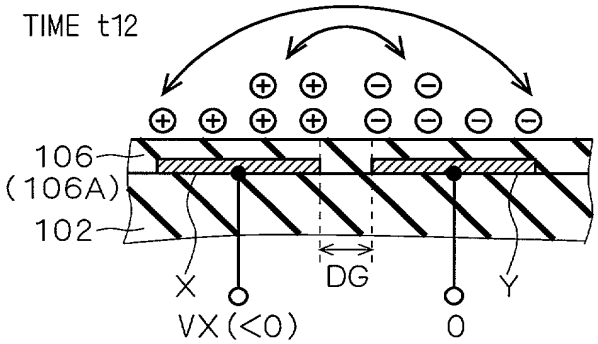


FIG. 11

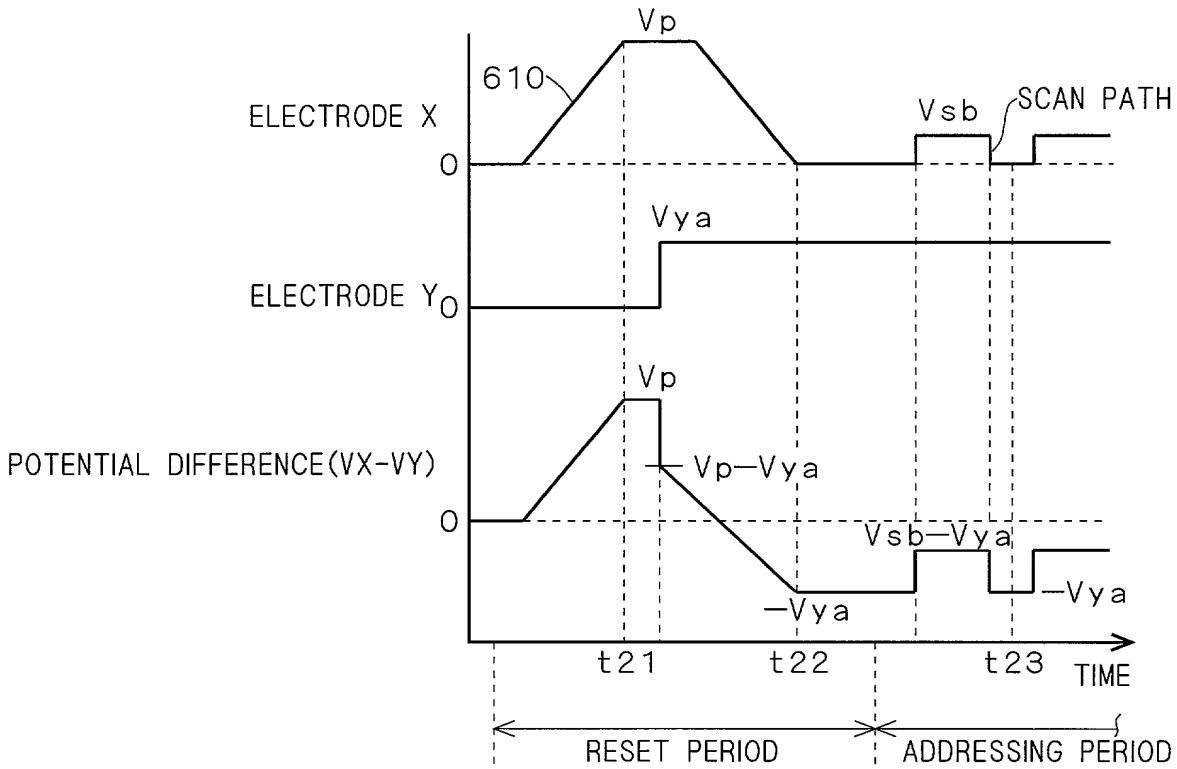

Vp
610
ELECTRODE X
0
Vsb
SCAN PATH
Vya
ELECTRODE Y
0
Vp
POTENTIAL DIFFERENCE(VX-VY)
Vp—Vya
0
Vsb—Vya
—Vya
—Vya
t21
t22
t23
TIME
RESET PERIOD
ADDRESSING PERIOD

FIG. 12

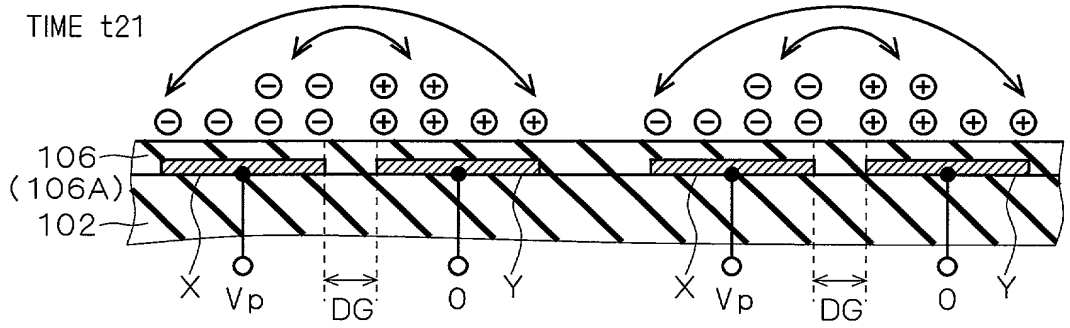

TIME t21
106
(106A)
102
X
Vp
DG
0
Y
X
Vp
DG
0
Y

FIG. 13

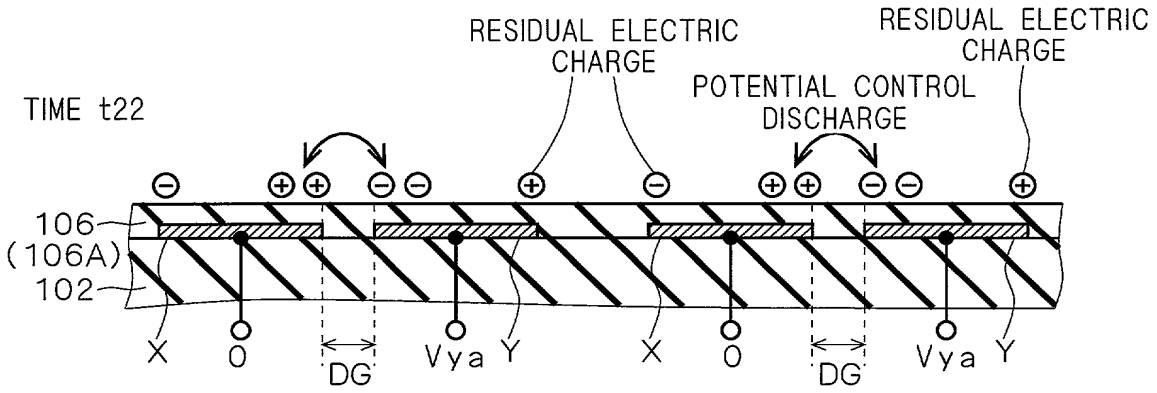

TIME t22
RESIDUAL ELECTRIC CHARGE
RESIDUAL ELECTRIC CHARGE
POTENTIAL CONTROL DISCHARGE
106
(106A)
102
X
0
DG
Vya
Y
X
0
DG
Vya
Y

FIG. 14

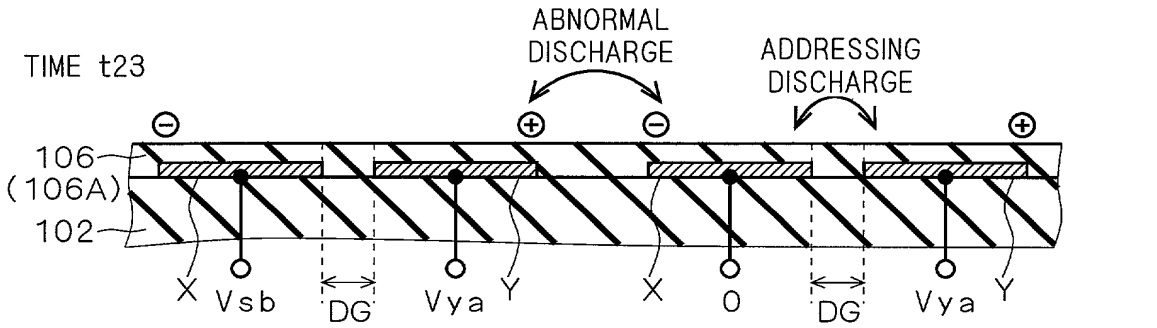

TIME t23
ABNORMAL DISCHARGE
ADDRESSING DISCHARGE
106
(106A)
102
X
Vsb
DG
Vya
Y
X
0
DG
Vya
Y

FIG. 15

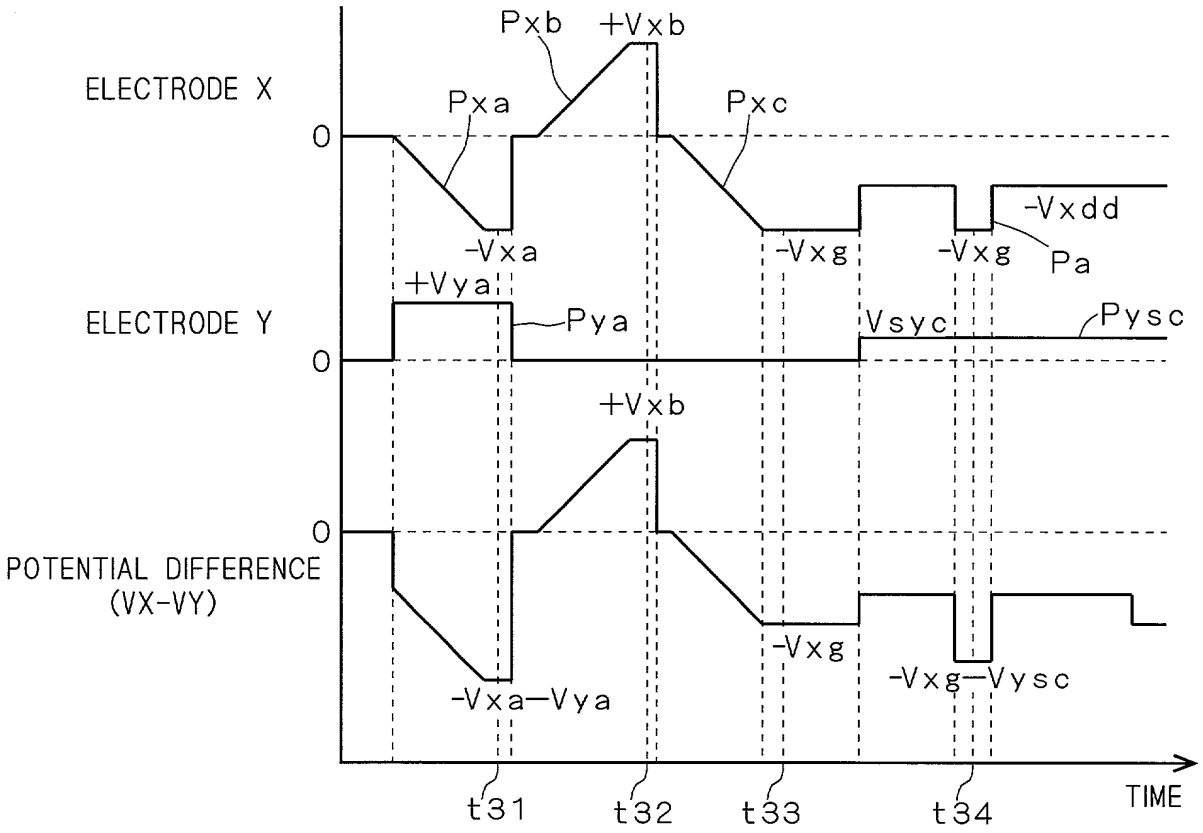

ELECTRODE X
Pxb
+Vxb
Pxa
Pxc
0
-Vxa
-Vxg
-Vxg
-Vxdd
Pa
+Vya
ELECTRODE Y
Pya
Vsyc
Pysc
0
+Vxb
0
POTENTIAL DIFFERENCE
(VX-VY)
-Vxg
-Vxg—Vysc
-Vxa—Vya
t31
t32
t33
t34
TIME

FIG. 16

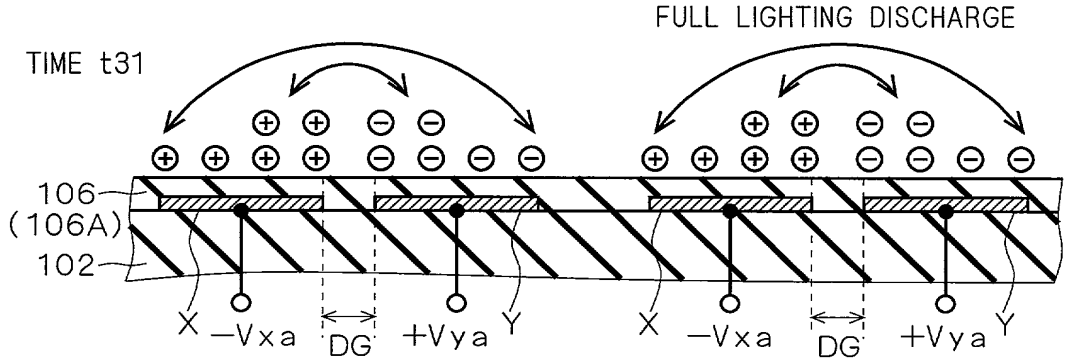

FULL LIGHTING DISCHARGE
TIME t31
106
(106A)
102
X
-Vxa
DG
+Vya
Y
X
-Vxa
DG
+Vya
Y

FIG. 17

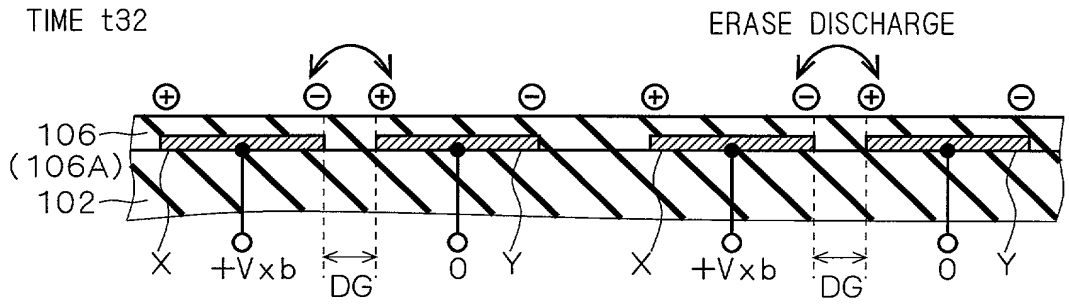


FIG. 18

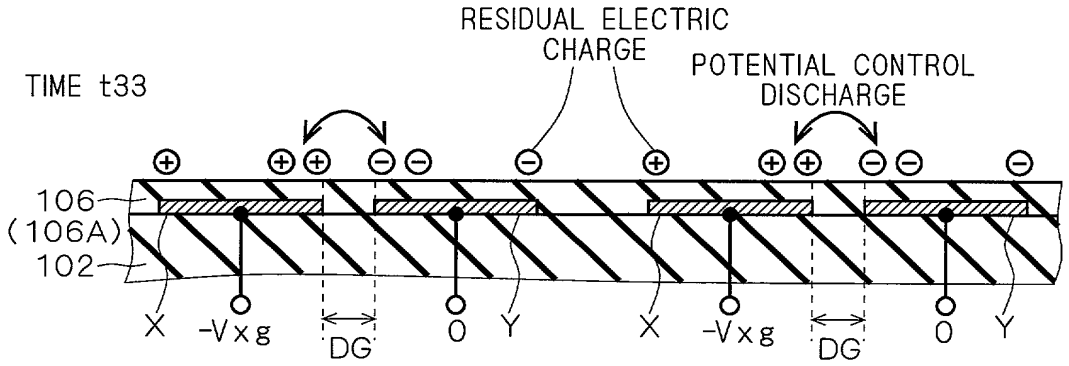


FIG. 19

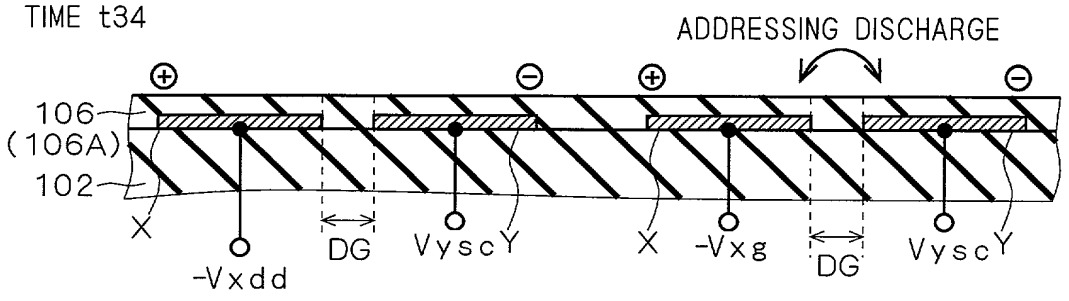


FIG. 20

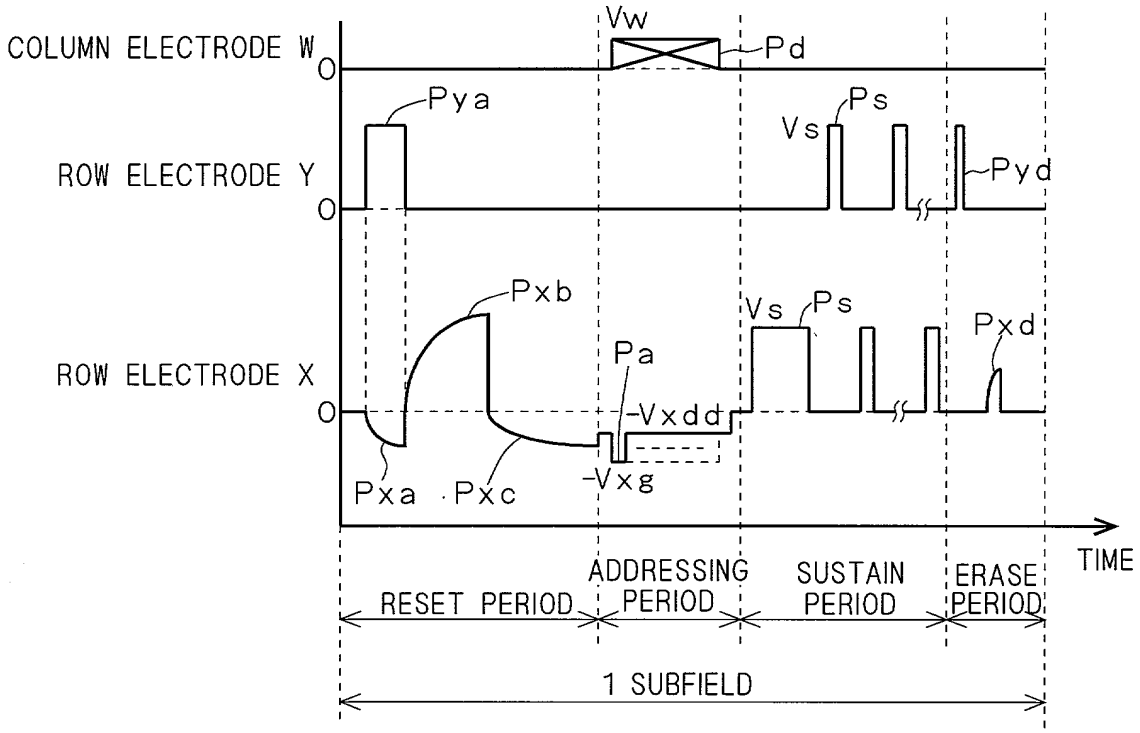

COLUMN ELECTRODE W
ROW ELECTRODE Y
ROW ELECTRODE X
0
Vw
Pd
Pya
Ps
Vs
Pyd
Pxb
Pa
-Vxdd
Pxd
Pxa
Pxc
-Vxg
TIME
RESET PERIOD
ADDRESSING PERIOD
SUSTAIN PERIOD
ERASE PERIOD
1 SUBFIELD

FIG. 21

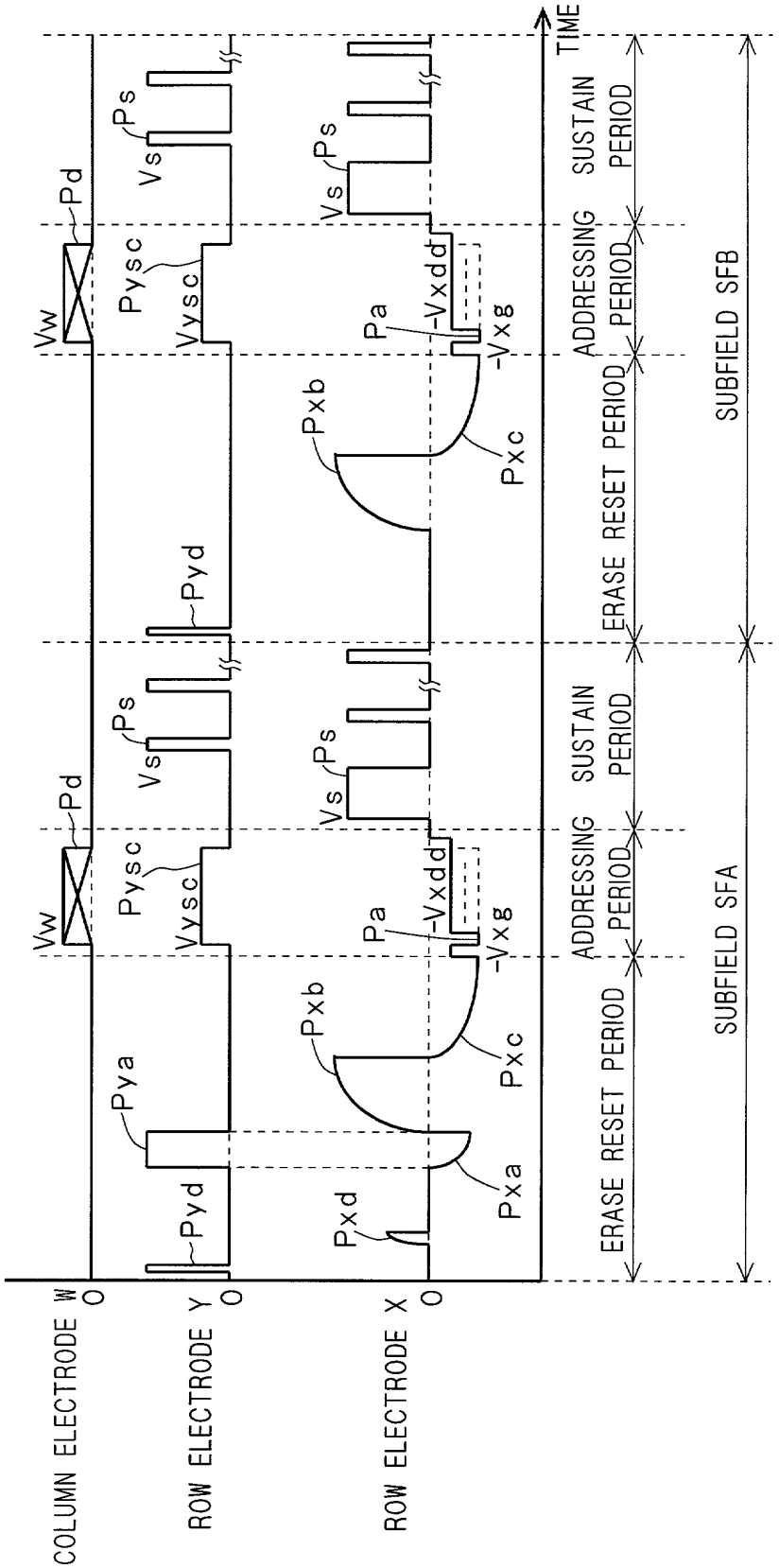

TIME
COLUMN ELECTRODE W
ROW ELECTRODE Y
ROW ELECTRODE X
0
Vw
Pd
Pysc
Vysc
Ps
Vs
Pyd
Pya
Pxd
Pxb
Pxc
Pxa
Pa
-Vxdd
-Vxg
ADDRESSING PERIOD
SUSTAIN PERIOD
ERASE RESET PERIOD
SUBFIELD SFB
SUBFIELD SFA

FIG. 22

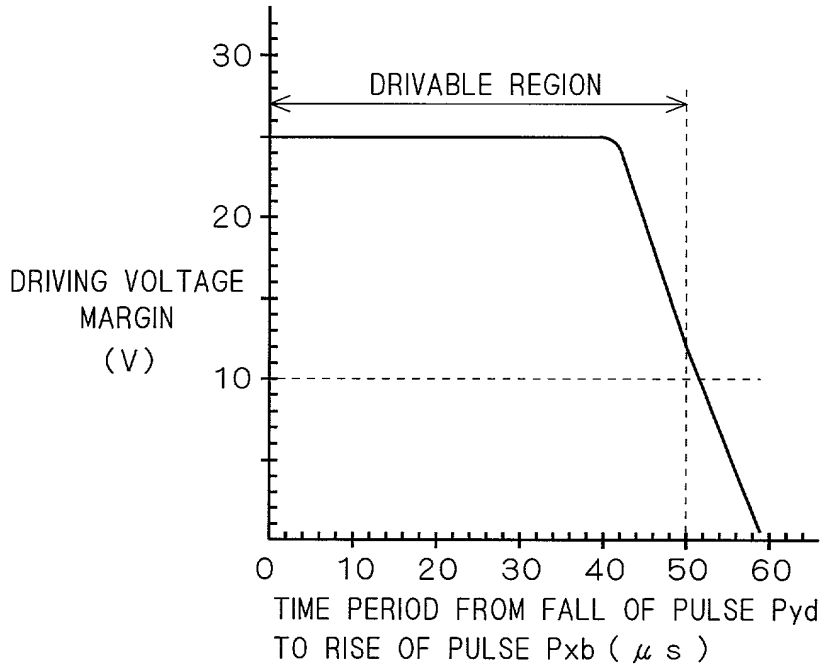

30
DRIVABLE REGION
20
DRIVING VOLTAGE MARGIN (V)
10
0
10
20
30
40
50
60
TIME PERIOD FROM FALL OF PULSE Pyd TO RISE OF PULSE Pxb (μ s)

FIG. 23

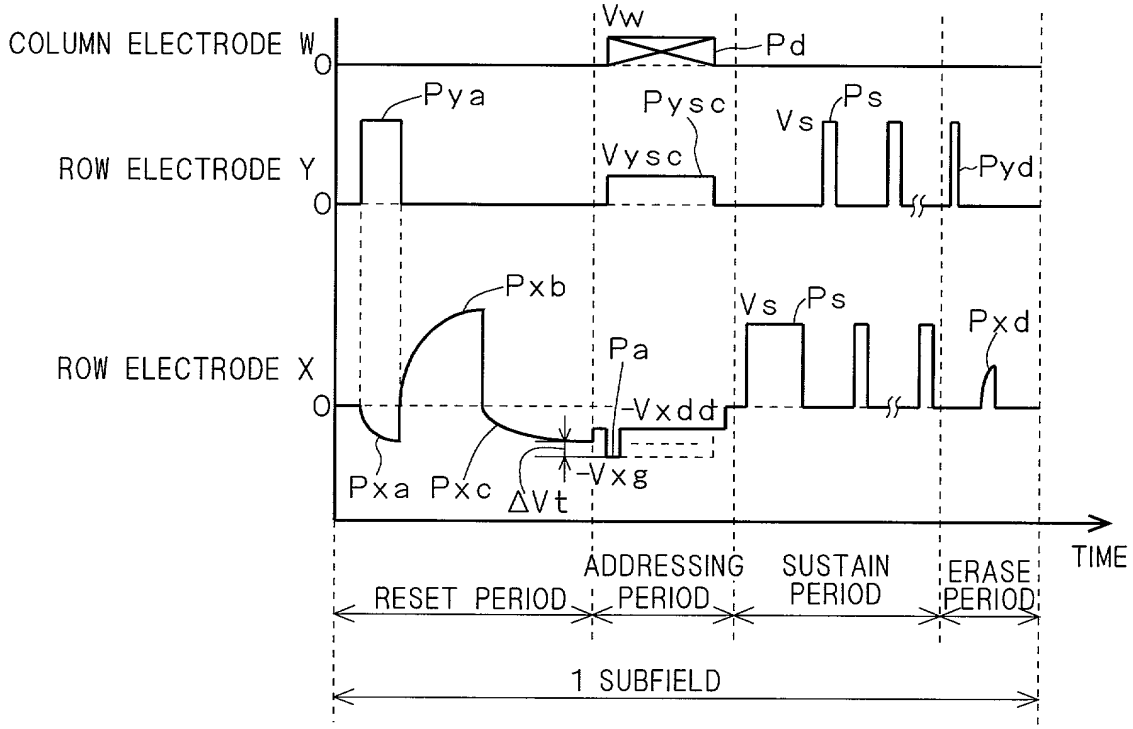

COLUMN ELECTRODE W
Vw
Pd
Pya
Pysc
Vs
Ps
ROW ELECTRODE Y
Vysc
Pyd
Pxb
Vs
Ps
Pxd
ROW ELECTRODE X
Pa
-Vxdd
Pxa
Pxc
ΔVt
-Vxg
TIME
RESET PERIOD
ADDRESSING PERIOD
SUSTAIN PERIOD
ERASE PERIOD
1 SUBFIELD

FIG. 24

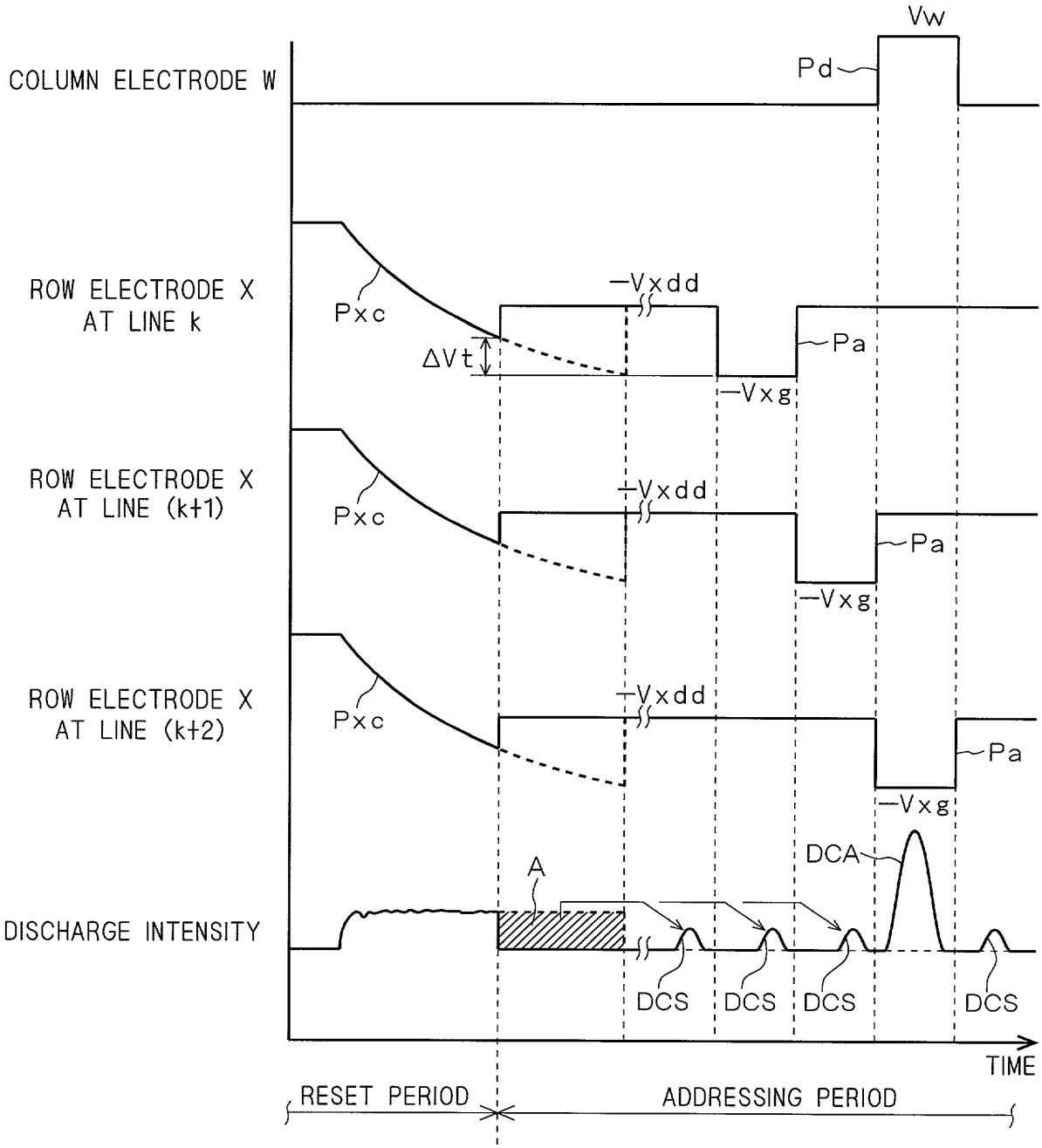

Vw
COLUMN ELECTRODE W
Pd
ROW ELECTRODE X AT LINE k
Pxc
-Vxdd
ΔVt
Pa
-Vxg
ROW ELECTRODE X AT LINE (k+1)
Pxc
-Vxdd
Pa
-Vxg
ROW ELECTRODE X AT LINE (k+2)
Pxc
-Vxdd
Pa
-Vxg
DISCHARGE INTENSITY
A
DCA
DCS
DCS
DCS
DCS
TIME
RESET PERIOD
ADDRESSING PERIOD

FIG. 25

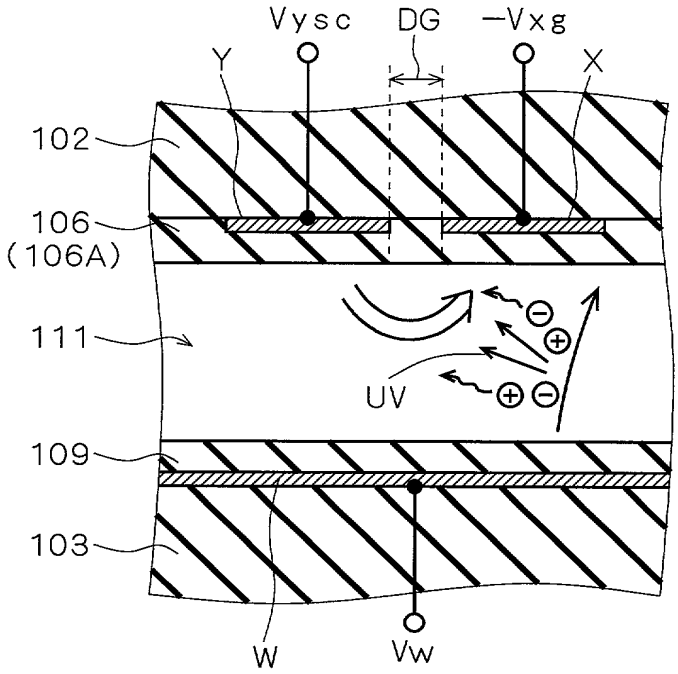

Vysc
DG
−Vxg
Y
X
102
106
(106A)
111
UV
109
103
W
Vw

FIG. 26

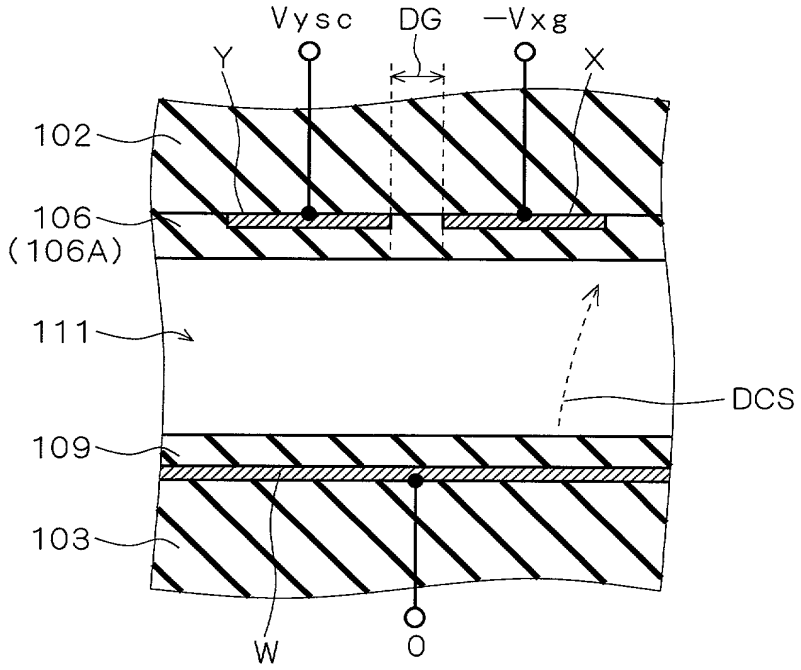
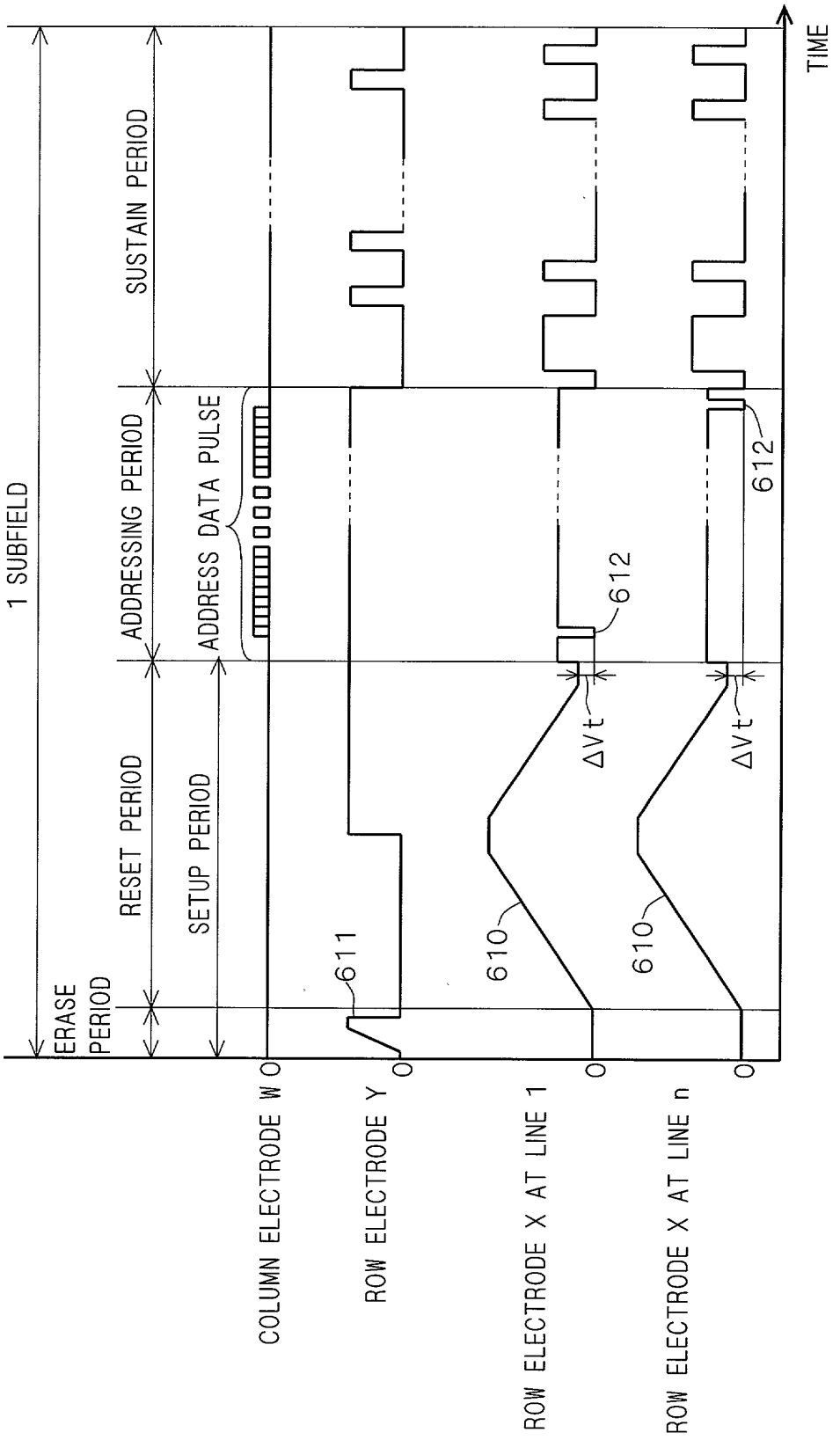

Vysc
DG
−Vxg
Y
X
102
106
(106A)
111
DCS
109
103
W
0

FIG. 27


1 SUBFIELD
ERASE PERIOD
RESET PERIOD
SETUP PERIOD
ADDRESSING PERIOD
ADDRESS DATA PULSE
SUSTAIN PERIOD
TIME
COLUMN ELECTRODE W
ROW ELECTRODE Y
ROW ELECTRODE X AT LINE 1
ROW ELECTRODE X AT LINE n
611
610
610
612
612
ΔVt
ΔVt
0
0
0
0

Tahara 20020220

FIG. 28

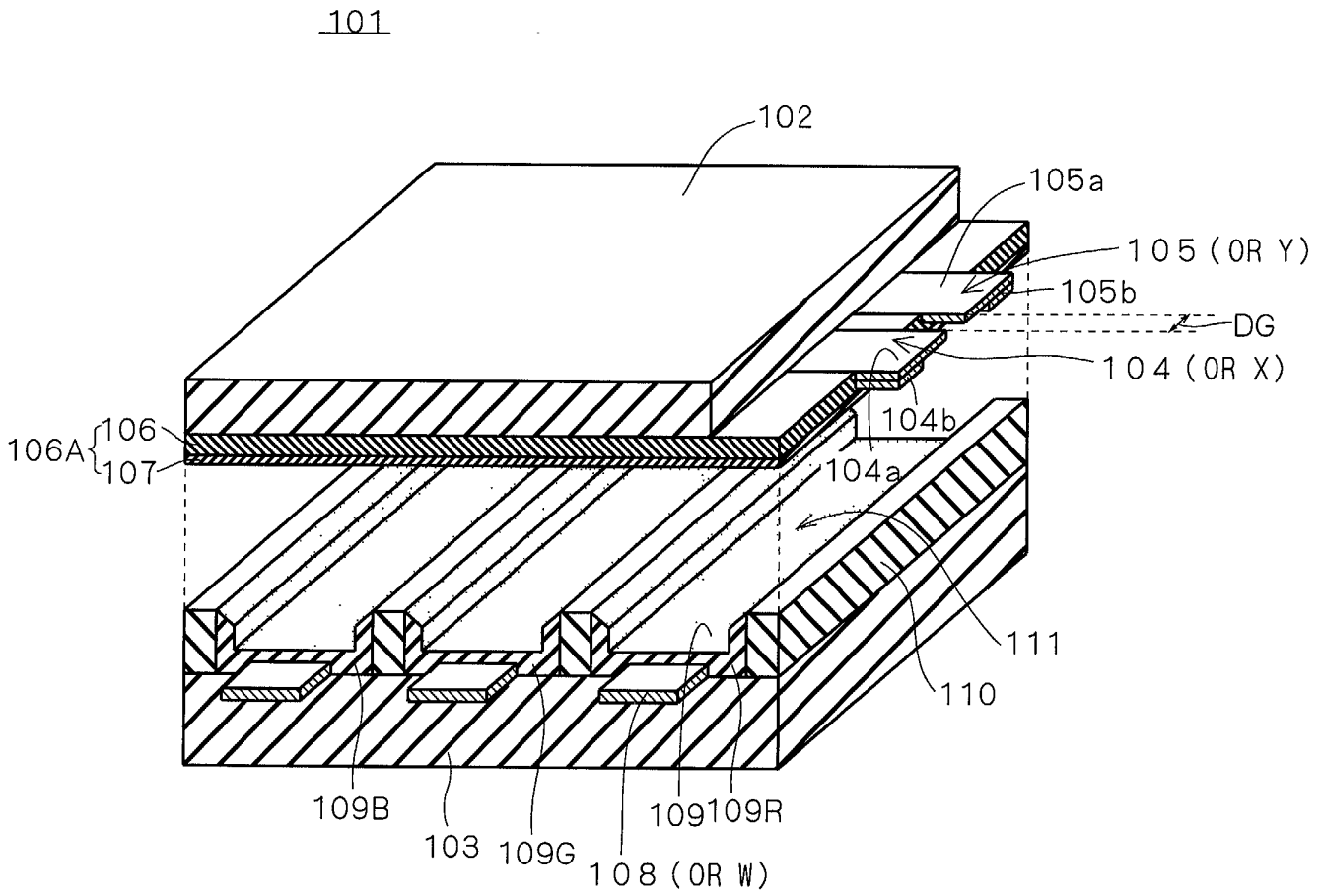


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FIG. 29

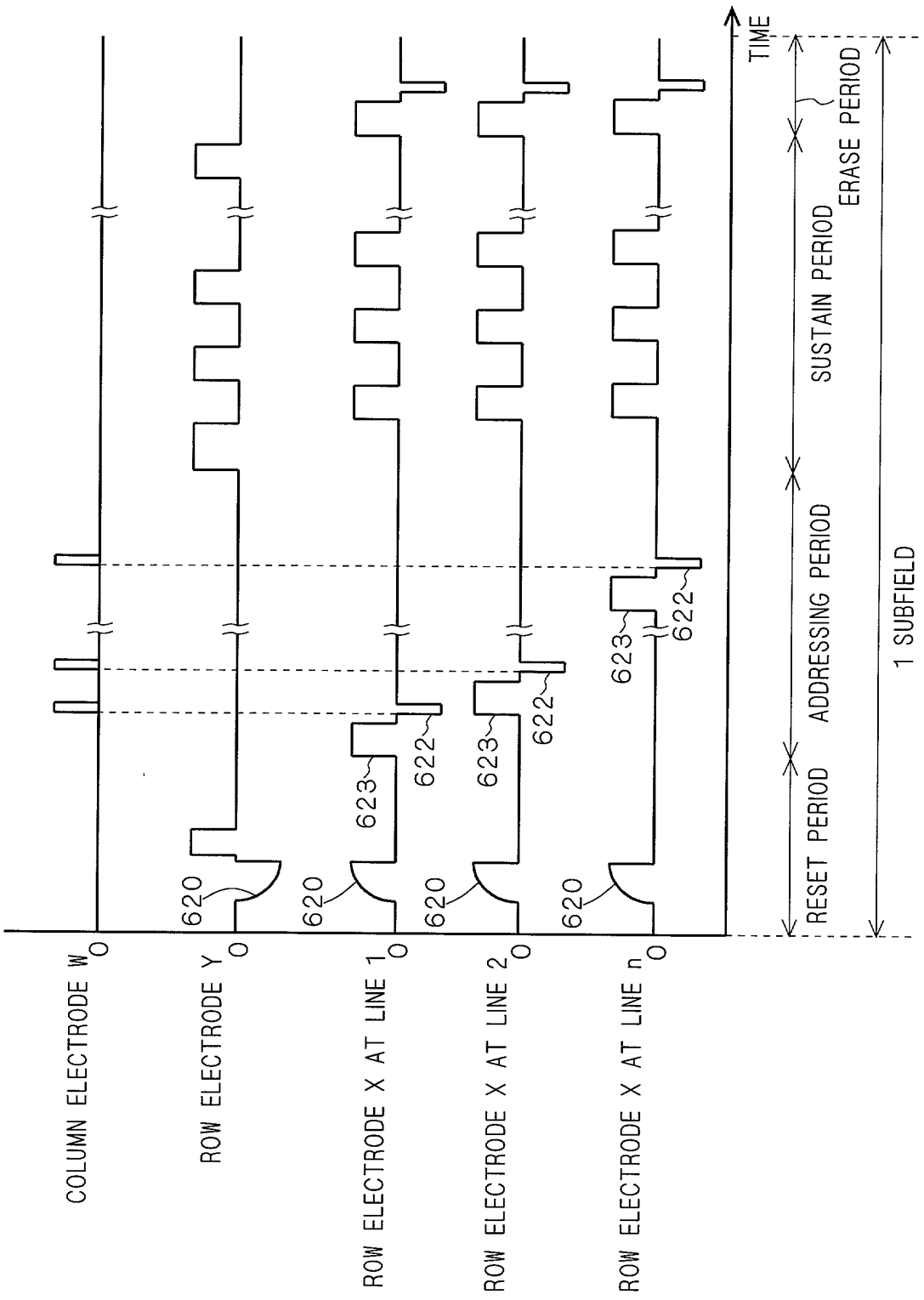
COLUMN ELECTRODE W
ROW ELECTRODE Y
ROW ELECTRODE X AT LINE 1
ROW ELECTRODE X AT LINE 2
ROW ELECTRODE X AT LINE n
620
623
622
TIME
RESET PERIOD
ADDRESSING PERIOD
SUSTAIN PERIOD
ERASE PERIOD
1 SUBFIELD

FIG. 30

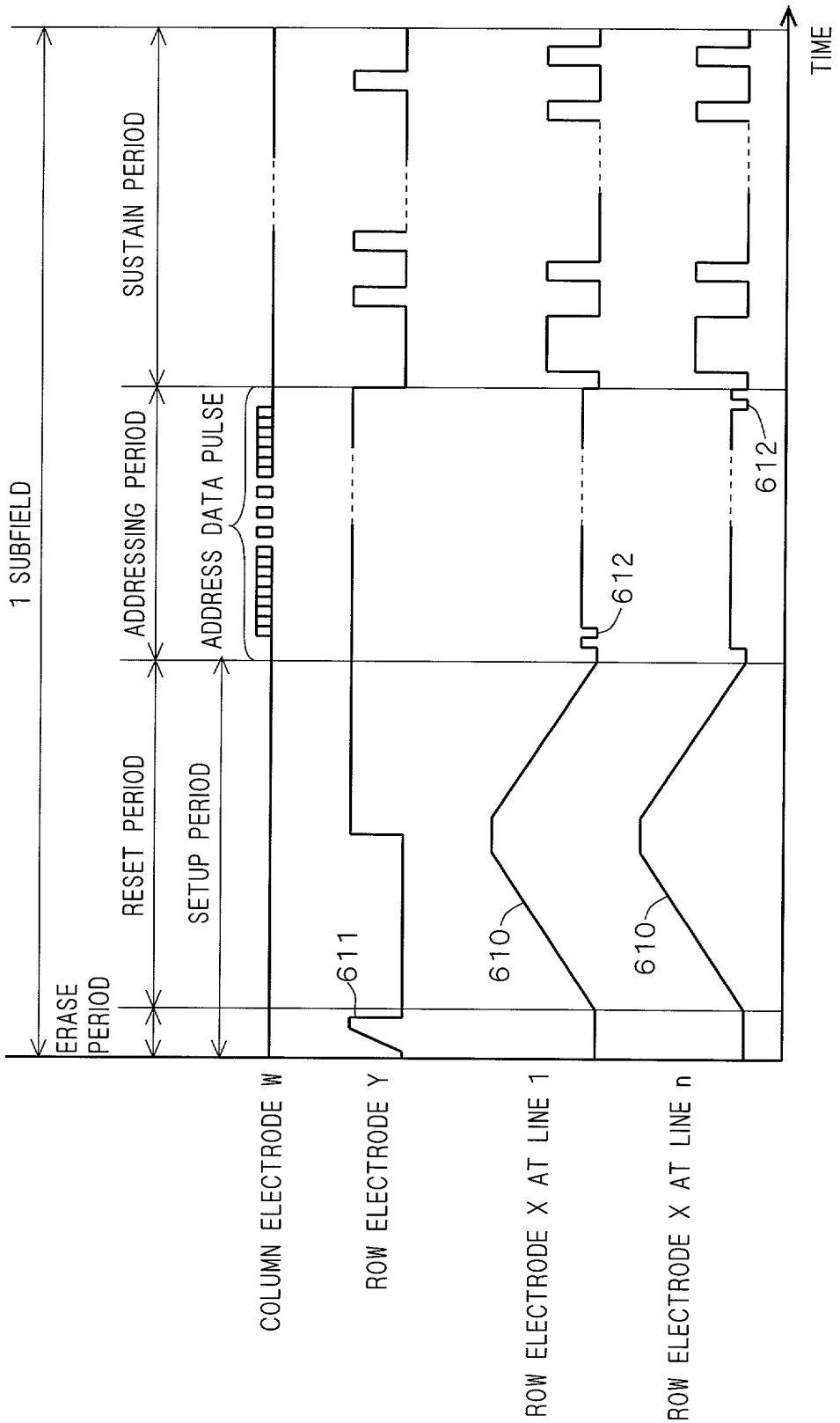
1 SUBFIELD
ERASE PERIOD
RESET PERIOD
SETUP PERIOD
ADDRESSING PERIOD
ADDRESS DATA PULSE
SUSTAIN PERIOD
TIME
COLUMN ELECTRODE W
ROW ELECTRODE Y
ROW ELECTRODE X AT LINE 1
ROW ELECTRODE X AT LINE n
611
610
610
612
612
612

FIG. 31

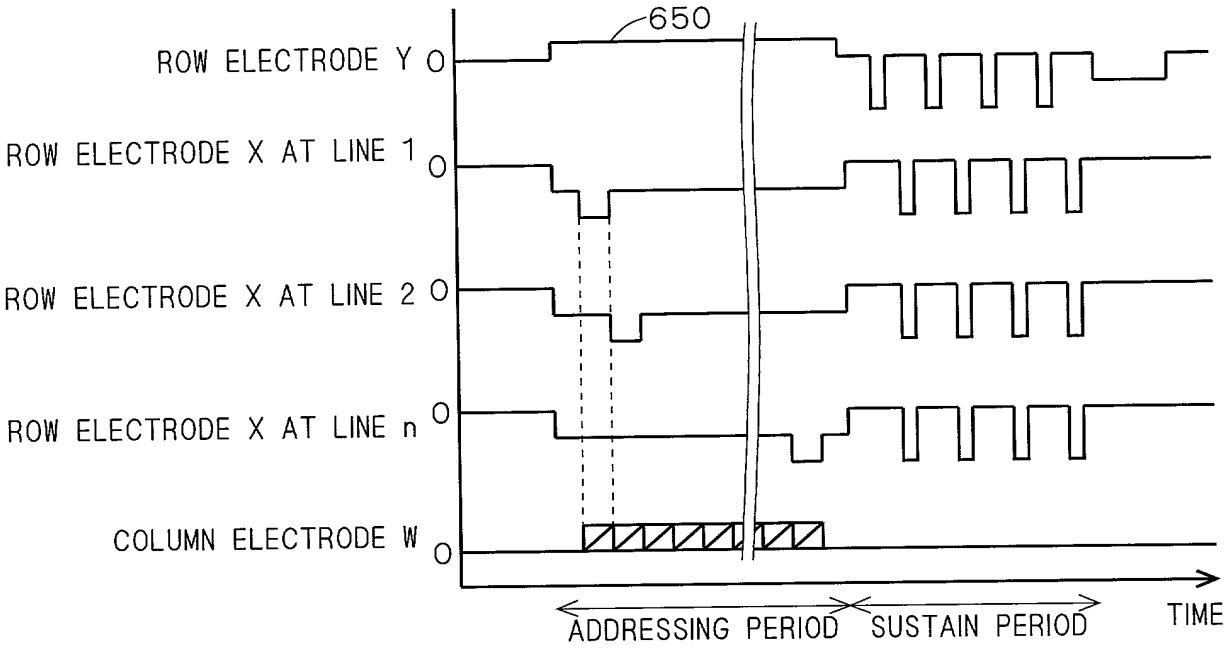
650
ROW ELECTRODE Y
ROW ELECTRODE X AT LINE 1
ROW ELECTRODE X AT LINE 2
ROW ELECTRODE X AT LINE n
COLUMN ELECTRODE W
O
ADDRESSING PERIOD
SUSTAIN PERIOD
TIME

FIG. 32

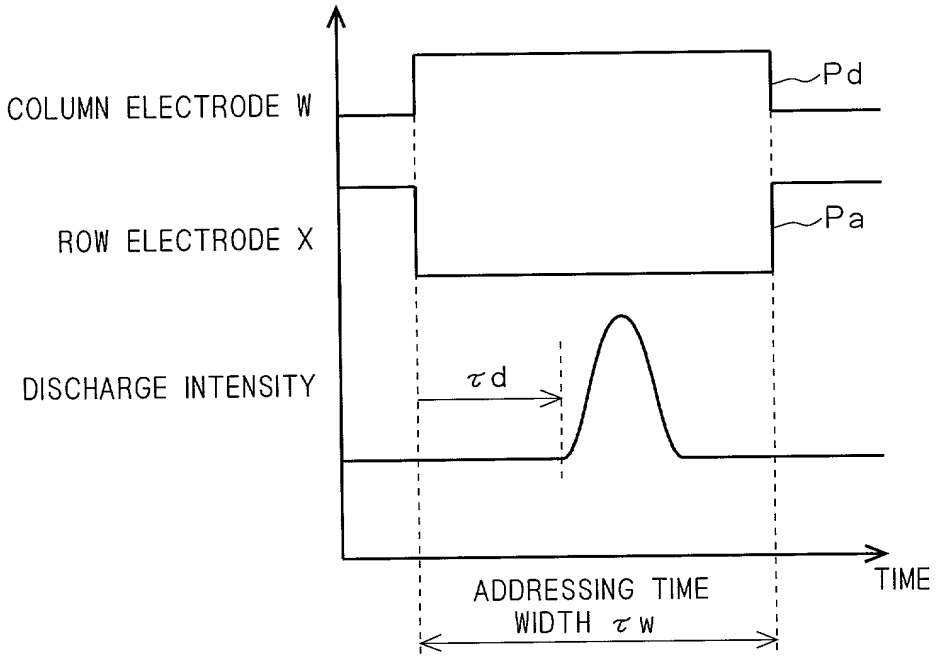
COLUMN ELECTRODE W
ROW ELECTRODE X
DISCHARGE INTENSITY
Pd
Pa
τd
ADDRESSING TIME
WIDTH τw
TIME

FIG. 33

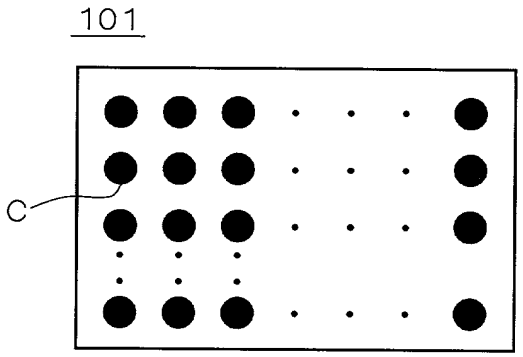

FIG. 34

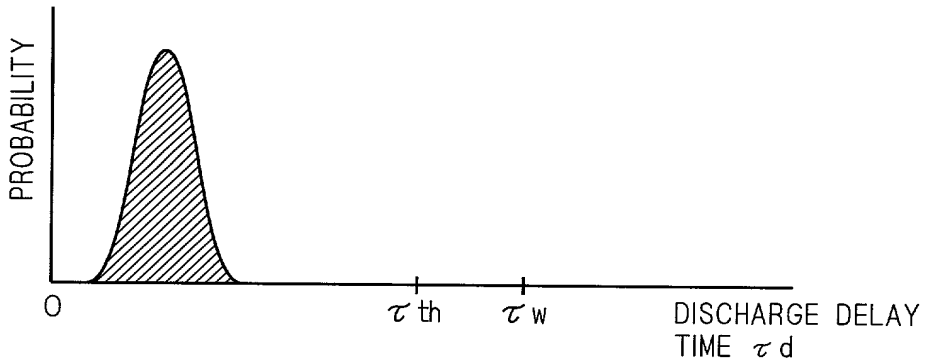

FIG. 35

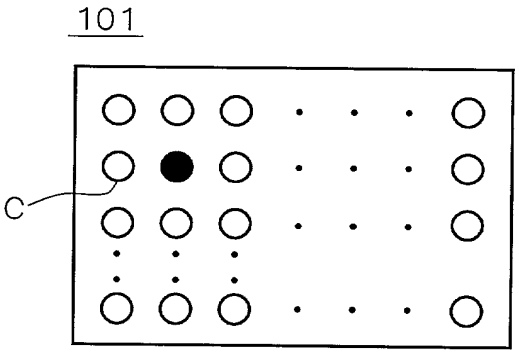

FIG. 36